Explore the next sense

A111 PCB Layout Guideline

A111 GND plane

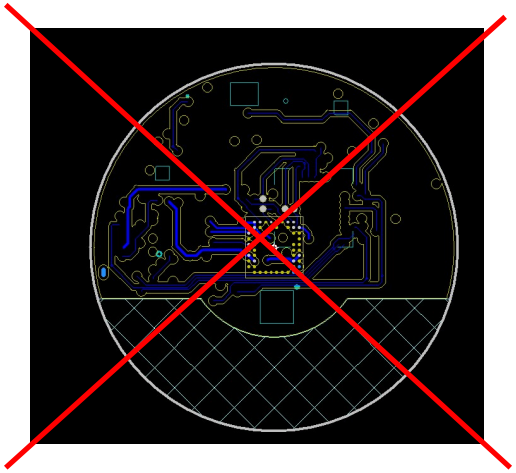
- Preferably no other components mounted on the same layer as A111. See A111 Sensor Integration Electromagnetic Scattering document for details:

https://developer.acconeer.com/download/user-guide-sensor-integration-electromagnetic-scattering-pdf/

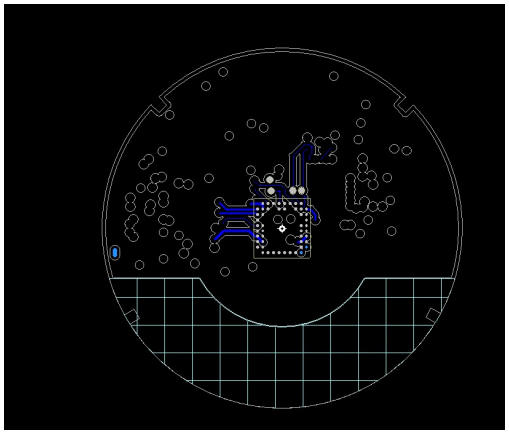
- GND plane on the same layer as A111. As few traces as possible breaking up the ground. Avoid creating GND islands
- Size of GND plane affects gain. See datasheet chapter 8 for details:

https://developer.acconeer.com/download/a111-datasheet-pdf/

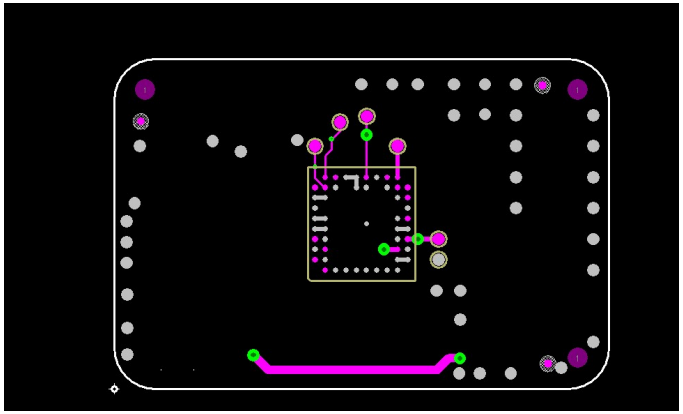
A111 GND plane examples



Not OK



Acceptable

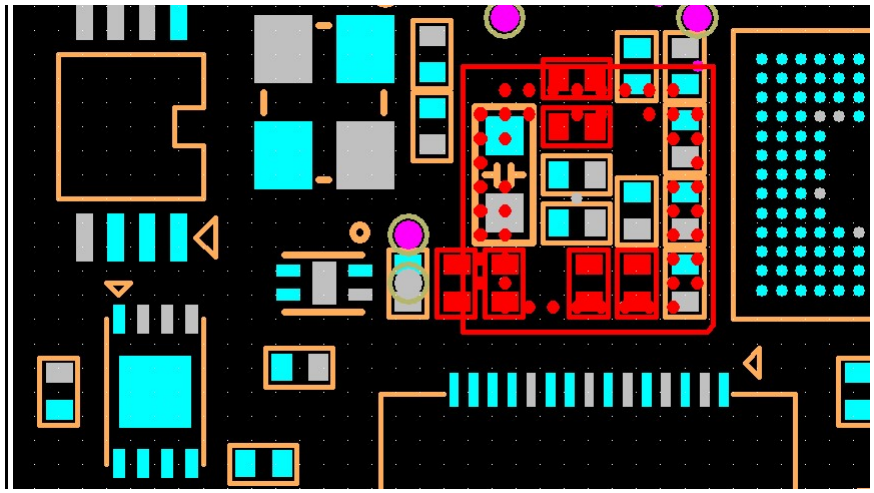


Very good

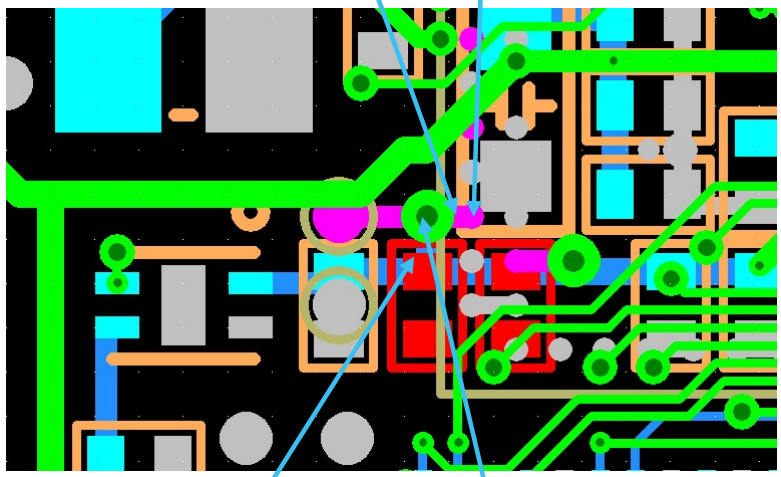
A111 capacitors

- Place the capacitors as close as possible to the A111 but on the opposite side of the PCB. Trace between capacitor and via and via and A111 ball as short as possible.

A111 capacitors - examples



A111 on Layer 1
Capacitors on Layer 4

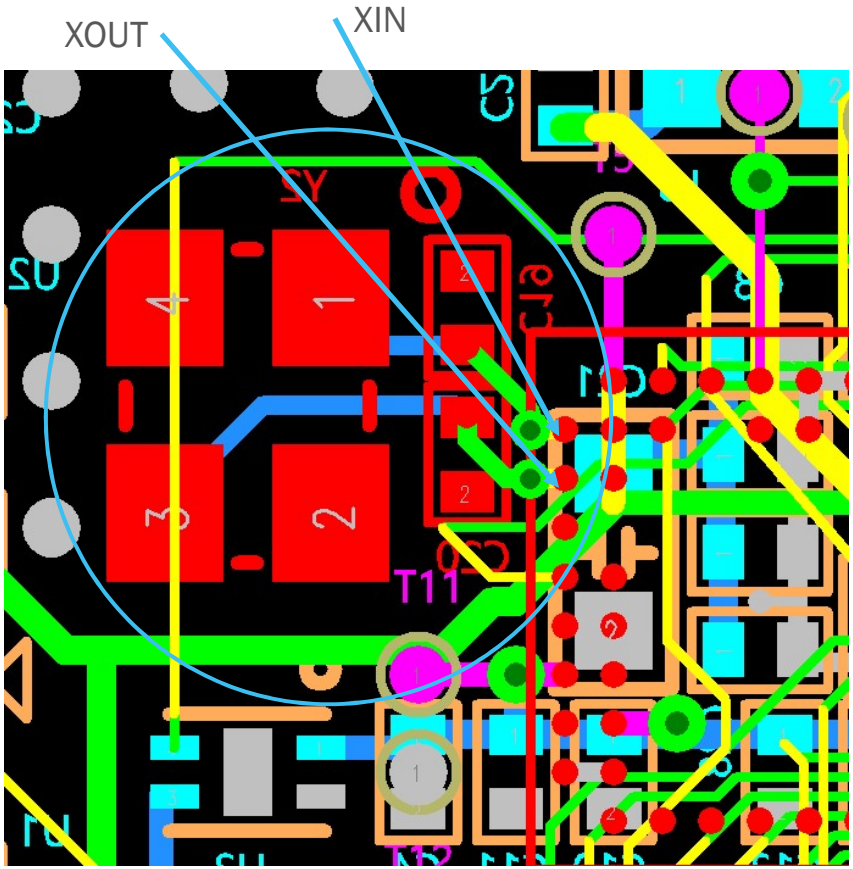


A111 crystal

- Place the crystal and its capacitors as close as possible to the A111 but on the opposite side of the PCB.
- Route the traces from the crystal and the capacitors to A111 with as few layer changes as possible.
- Capacitors should be placed between crystal pad and A111 ball.
- Make trace between capacitor and via and via and A111 ball as short as possible.
- Keep other traces away from the crystal traces.

A111 crystal - example

Example on 4-layer PCB:
Blue = Layer 4 traces
Green = Layer 3 traces
Yellow = Layer 2 traces
Purple = Layer 1 traces
A111 is on Layer 1
Crystal + capacitors are on Layer 4



A111 SPI interface – PCB layout

- Route SPI traces with GND above and below if possible. (If routed on inner layer). The signals are noisy.
- Make the traces as short as possible.
- Change layer as few times as possible.
- Route CLK, MISO and MOSI symmetrically if possible.
- Try to only cross other signals on adjacent layers at 90 degree angle. Do not route other signals in parallel with the SPI signals on the same layer or adjacent layers.

A111 SPI interface – PCB layout

- 30 Ohm resistor on MISO signal should be placed as close to the A111 ball as possible. It compensates for the fact that the A111 pad doesn't have 50 ohm impedance. Make trace between resistor and via and via and A111 ball as short as possible. If a capacitor is added, it should be as close to the 30 Ohm resistor as possible.
- In the case of MOSI and CLK, the resistor and capacitor should be placed as close to the MCU pin as possible.

A111 SPI interface PCB layout - examples

SPI CLK, MOSI, MISO (highlighted in red)
Are mainly routed on layer 2
Components except A111 on
layer 4.
Resistor on MISO placed close
to pin (highlighted in red).

Example on 4-layer PCB:
Blue = Layer 4 traces
Green = Layer 3 traces
Yellow = Layer 2 traces
Purple = Layer 1 traces